MOS Layer

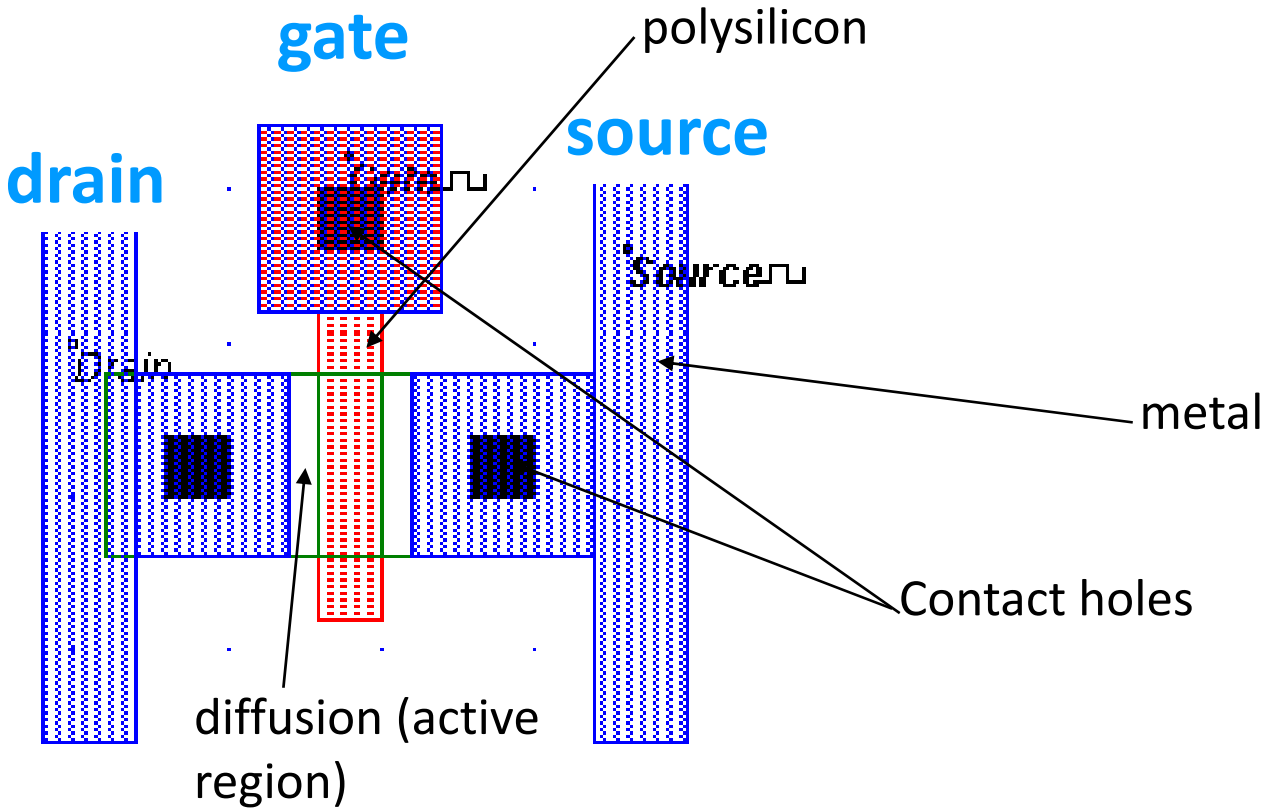
MOS Layer

- MOS design is aimed at turning a specification into masks for processing silicon to meet the specification.
- We have seen that MOS circuits are formed on four basic *layers-n-diffusion, p-diffusiqn, polysilicon, and metal, which are isolated from one another by thick or thin* (thinox) silicon dioxide insulating layers.

Mask Layout (*Print this presentation in colour if possible, otherwise highlight colours*)

- Circuit coloured mask layer layout
- Coloured stick diagram mask representation
- Lambda and layout design rules
- Mask layout of nMOS and CMOS inverters
- Mask layout of CMOS circuits (examples)
- Reading & understanding mask layout (exercises)

nMOS transistor mask representation



Mask layout & coloured stick diagram notation

Silicon layers are typically colour coded as follows :

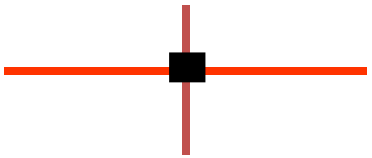
- diffusion (device well, local interconnect)
- polysilicon (gate electrode, interconnect)
- metal (contact, interconnect)
- contact windows
- depletion implant
- P well (CMOS devices)

This colour representation is used during mask layer definition

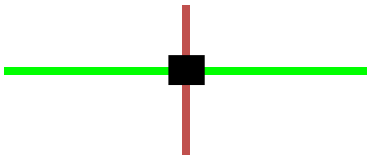
Translation from circuit format to a mask layout (and vice-versa) is relatively straightforward

Layer contact mask layout representation

A transistor is formed when device well is crossed by polysilicon.
Device well oxide : thin gate oxide

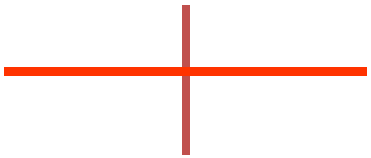


Metal contacting polysilicon

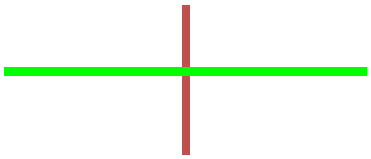


Metal contacting diffusion

- diffusion
- polysilicon
- metal
- contact windows
- depletion implant
- P well



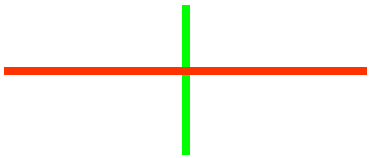
Metal crossing polysilicon (no contact, electrically isolated with thick oxide and so can carry separate voltages)



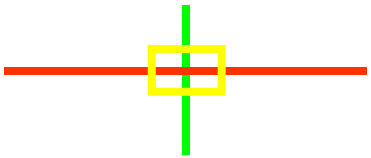
Metal contacting diffusion (no contact, electricall isolated with thick oxide)

Transistor mask layout representation

A transistor is formed when device well is crossed by polysilicon.
Device well oxide : thin gate oxide



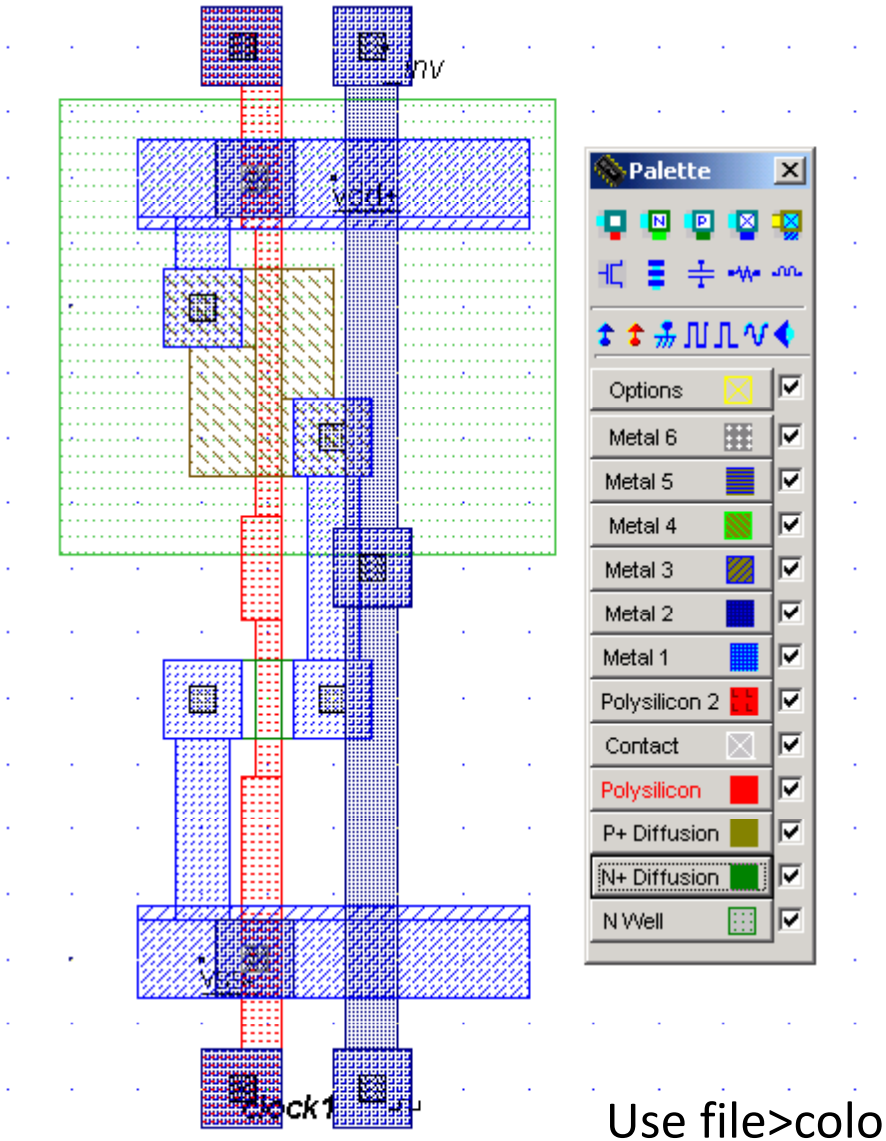
Enhancement mode transistor ($V_{th} \approx 0.2V_{dd}$)



Depletion mode transistor (extra well implant to provide $V_{th} \approx -0.6V_{dd}$)

- diffusion
- polysilicon
- metal
- contact windows
- depletion implant
- P well

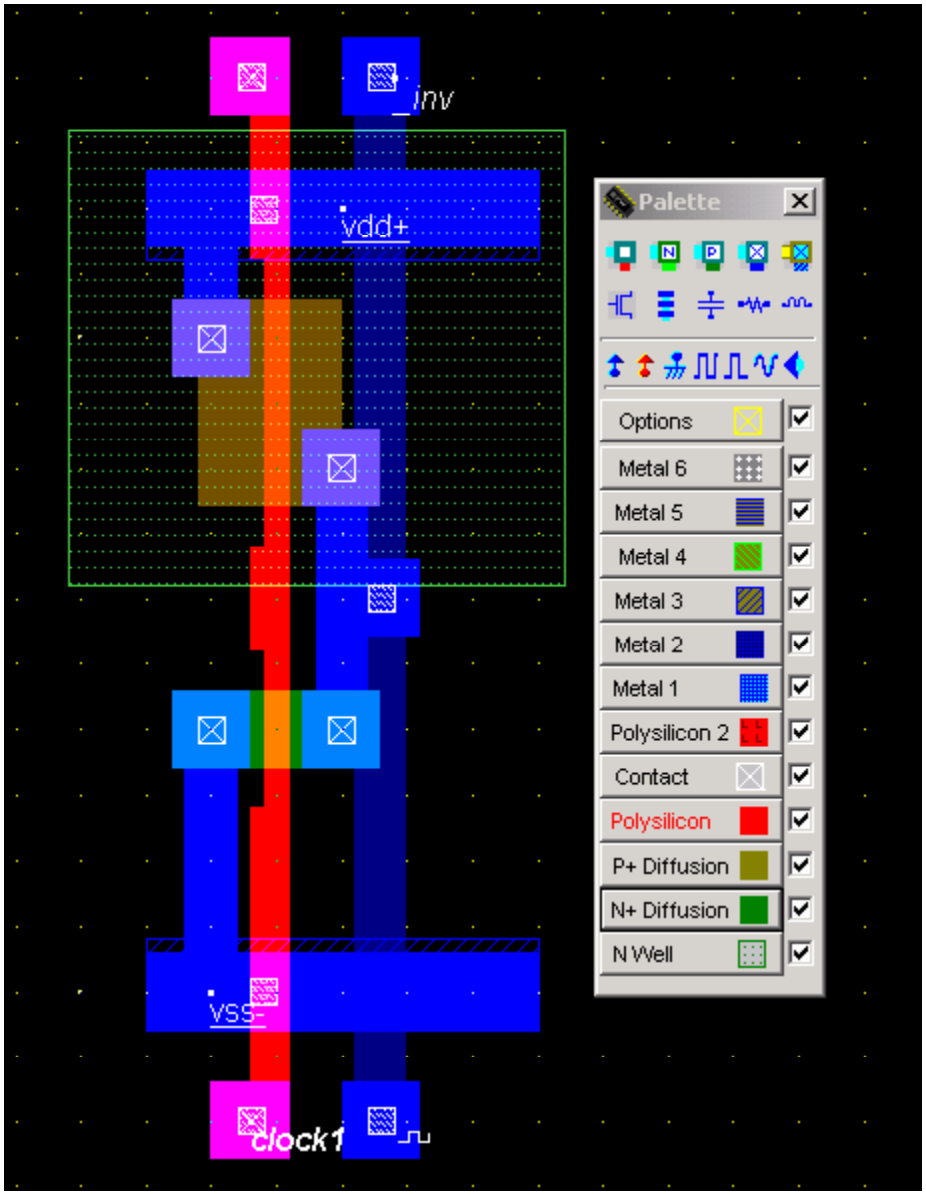
CMOS Inverter Mask Layout (using Microwind)



- diffusion
- polysilicon
- metal
- contact windows
- depletion implant
- P well

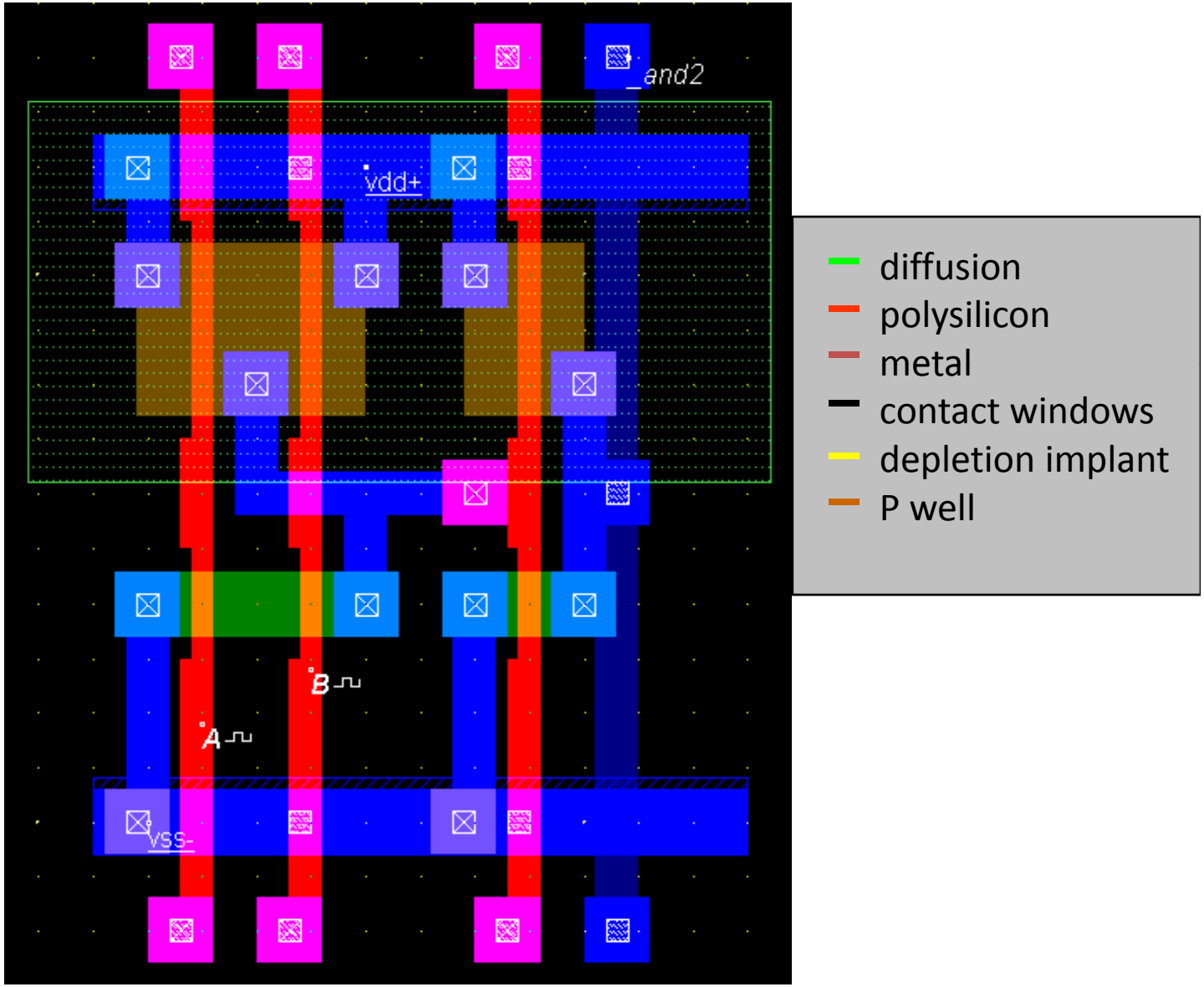
Use file>colors>white background

CMOS Inverter Mask Layout



- diffusion
- polysilicon
- metal
- contact windows
- depletion implant
- P well

CMOS AN2 (2 i/p AND gate) Mask Layout



Layout Design rules & Lambda (λ)

Lambda (λ) : distance by which a geometrical feature or any one layer may stay from any other geometrical feature on the same layer or any other layer.
All processing factors are included plus a safety margin.

λ used to prevent IC manufacturing problems due to mask misalignment or exposure & development variations on every feature, which otherwise could lead to :

- over-diffusion
- over-etching
- inadvertent transistor creation etc

λ is the minimum dimension which can be accurately re-produced on the silicon wafer for a particular technology.

Layout Design rules & Lambda (λ)

Minimum photolithographic dimension (width, not separation) is 2λ.
Hence, the minimum channel length dimension is 2λ.
Where a 0.25μm gate length is quoted, λ is 0.125 microns (μm).

Minimum distance rules between device layers, e.g.,

- polysilicon $\leftrightarrow$ metal
- metal $\leftrightarrow$ metal
- diffusion $\leftrightarrow$ diffusion and
- minimum layer overlaps

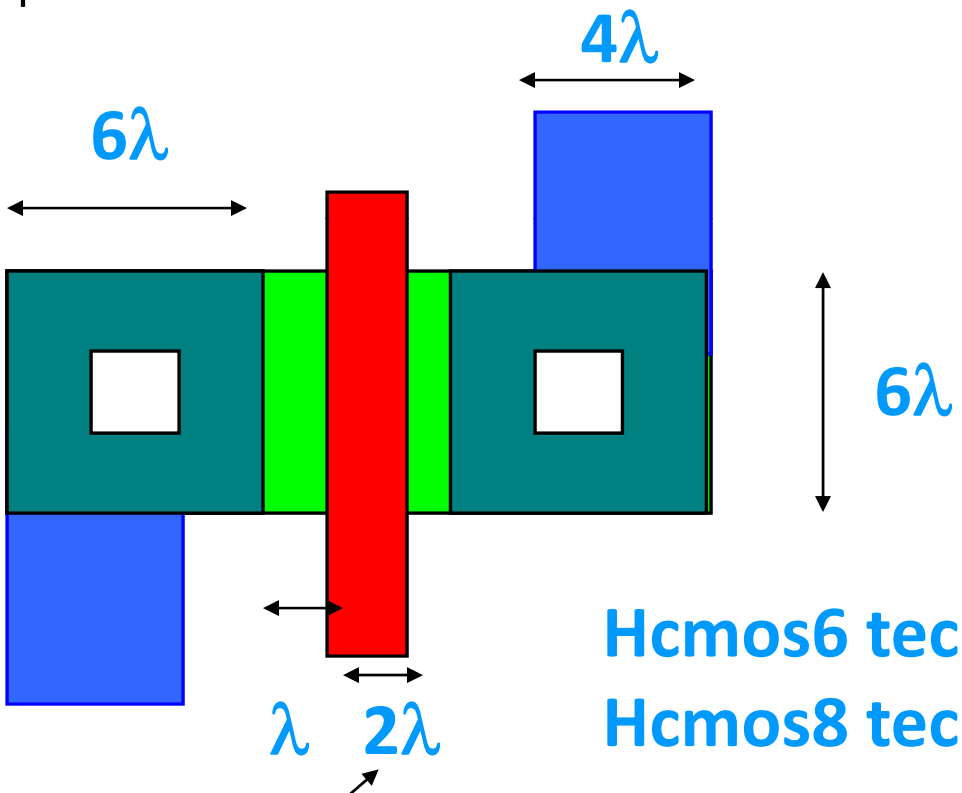
are used during layout

Layout design rule checker (DRC) automatically verifies that no design rules have been broken

Note however, the use of Lambda is not optimal but supports ***design reuse***

Layout Design rules & Lambda (λ)

Lambda based design: half of technology since 1985. As technology changes with smaller dimensions, a simple change in the value of λ can be used to produce a new mask set.

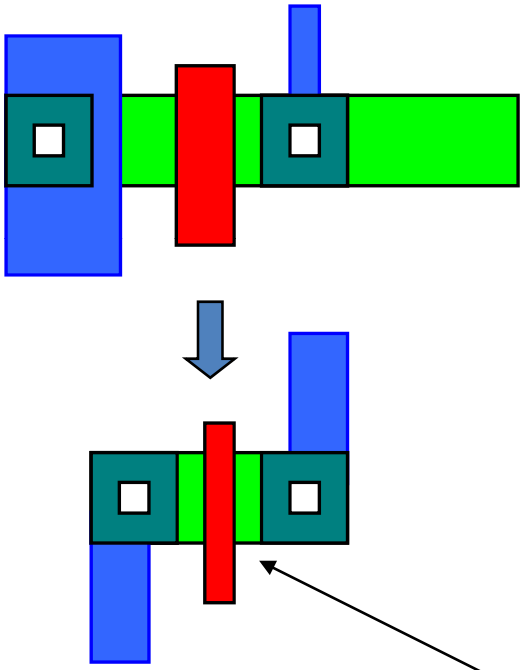


Hcmos6 technology : λ=0.2µm

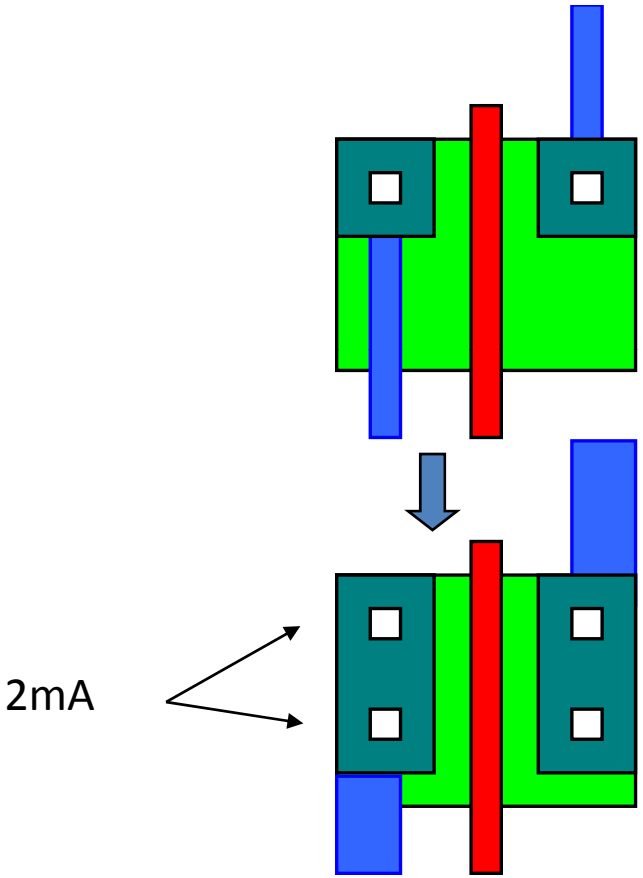
Hcmos8 technology : λ=0.1µm

All device mask dimensions are based on multiples of λ, e.g., polysilicon minimum width = 2λ. Minimum metal to metal spacing = 3λ

Basic design rules

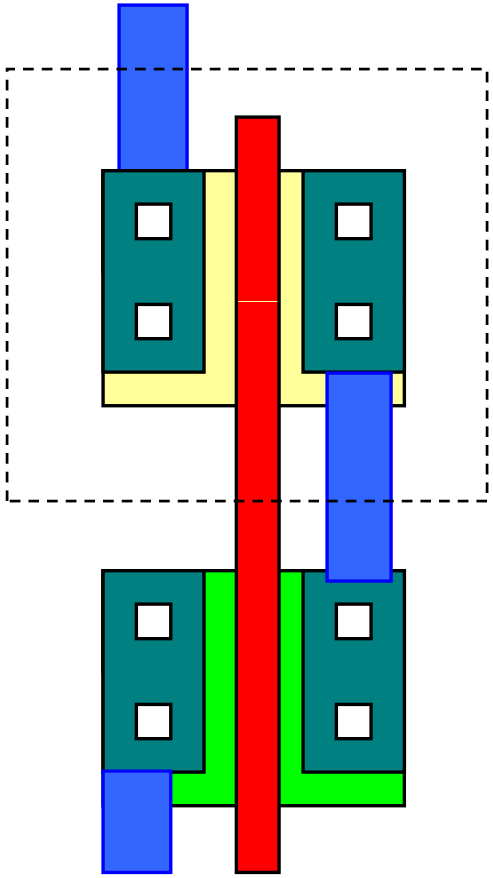


- Minimize spared diffusion
- Use minimum poly width (2λ)

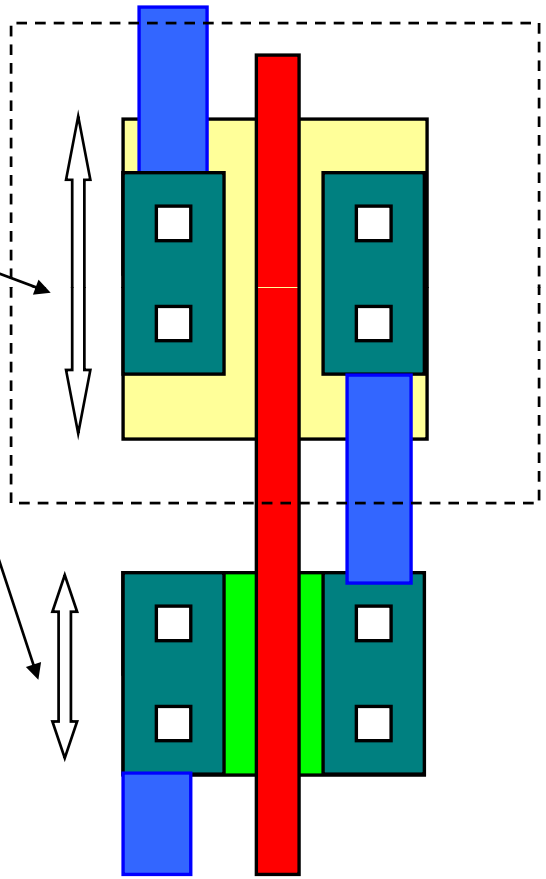


- 1 contact = 1mA
- Multiply contacts

Basic design rules



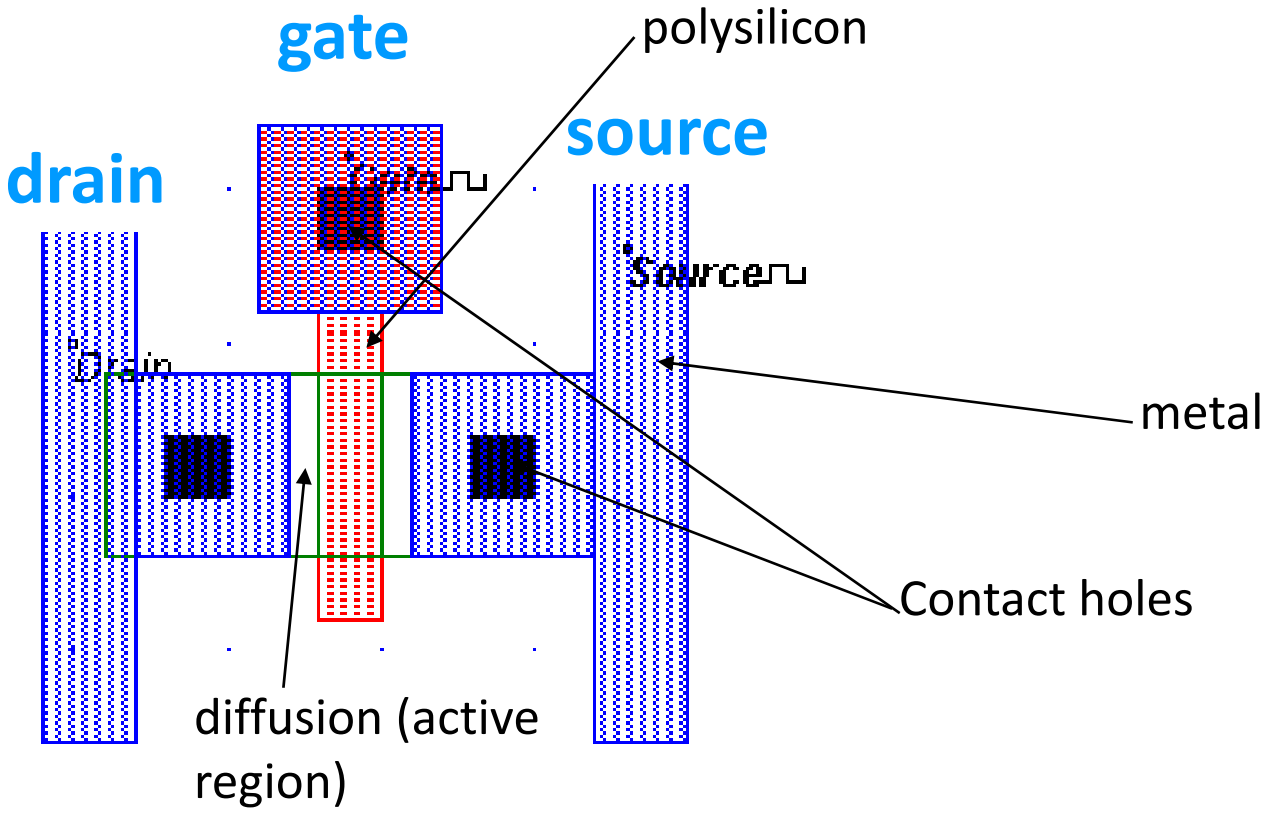
Width of pMOS should be twice the width of nMOS



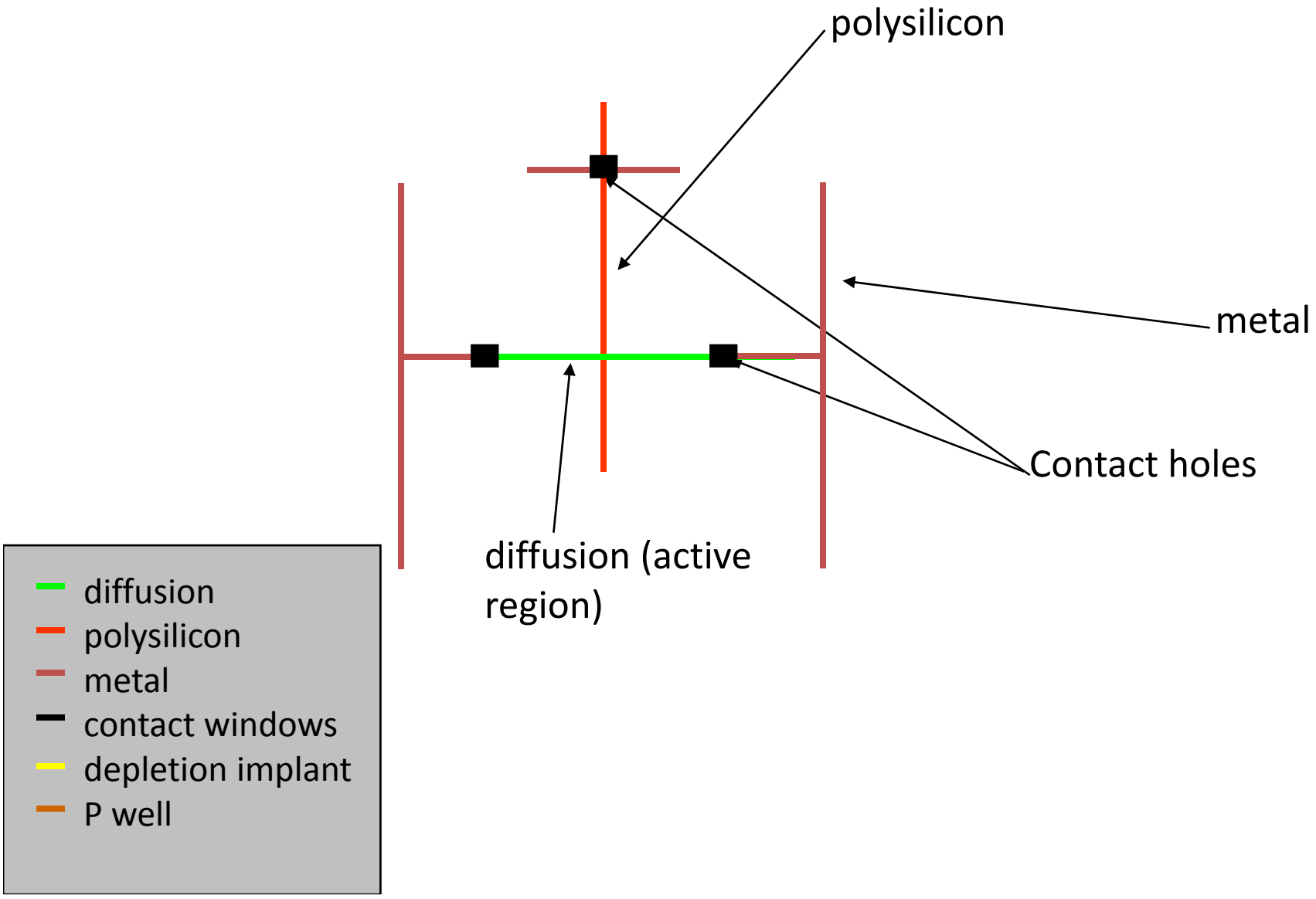
- Same N and P alters symmetry

- L min
- Wpmos=2 Wnmos

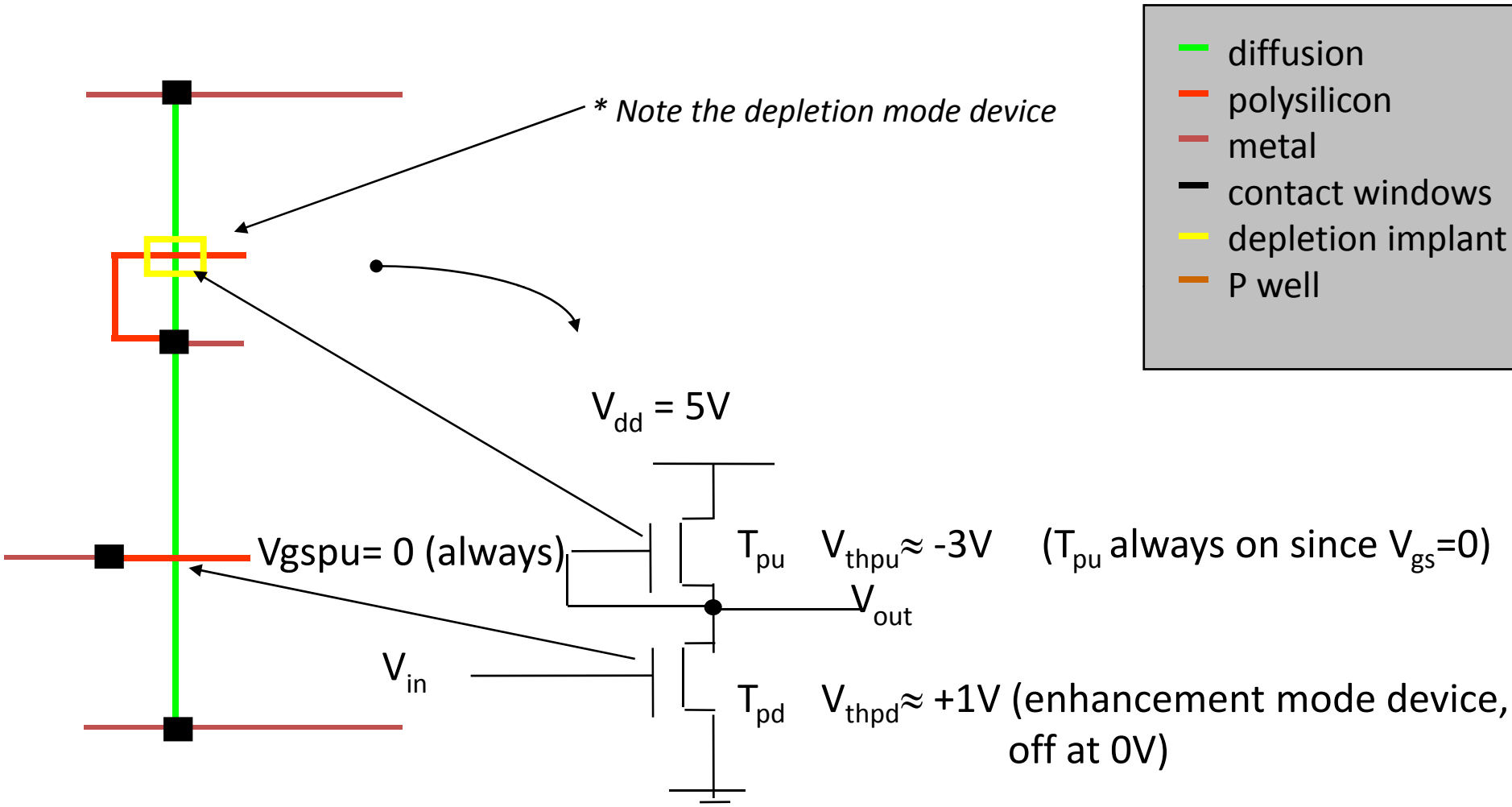
nMOS transistor mask representation (See stick diagram next slide) for comparison



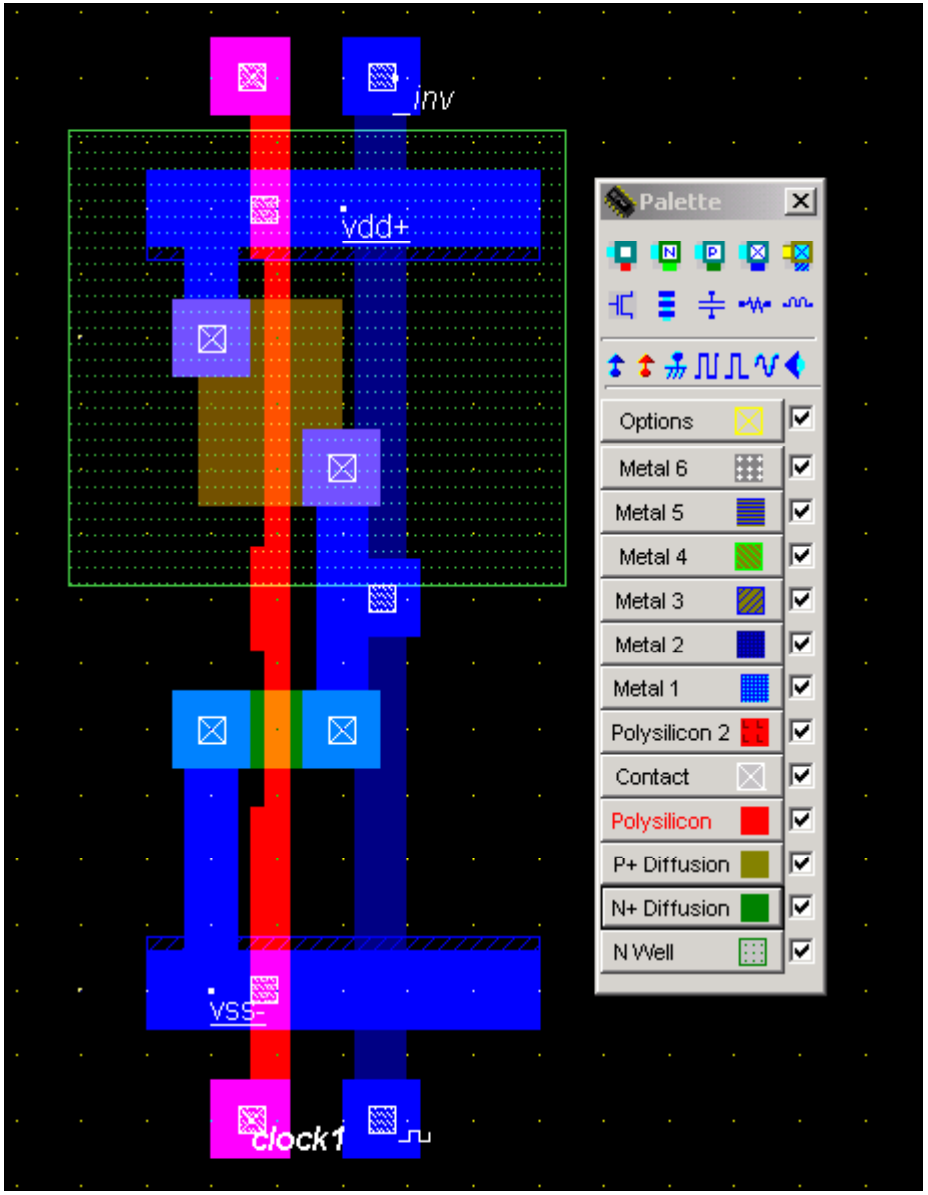
nMOS transistor coloured stick diagram representation



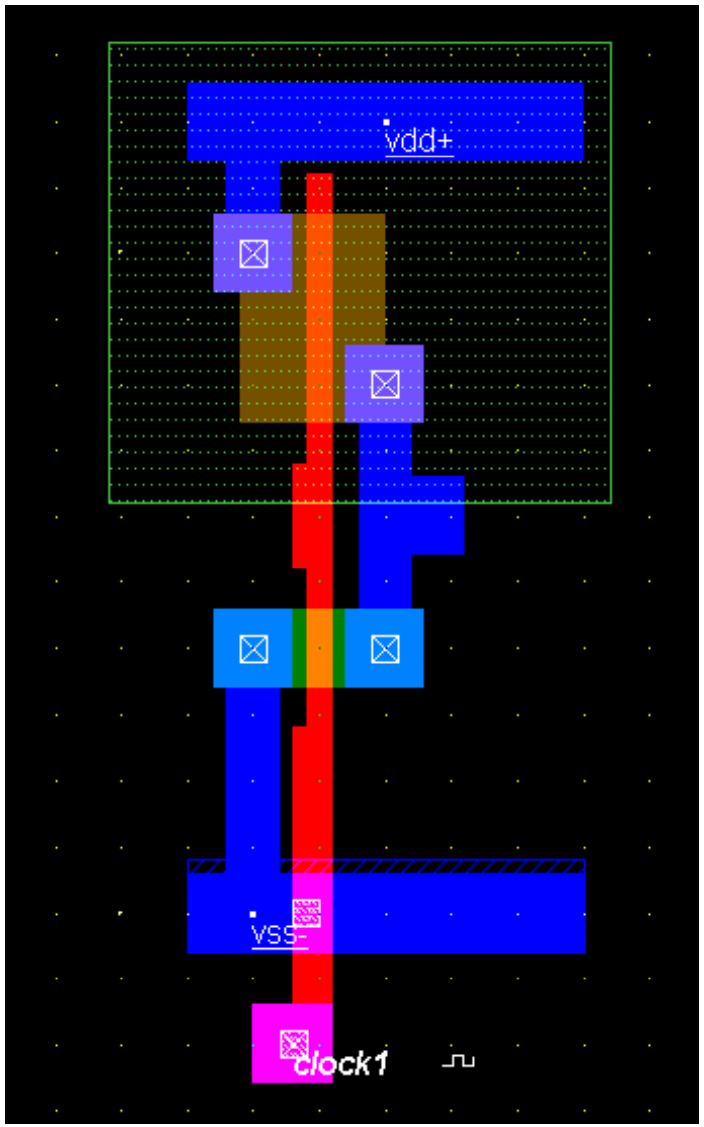
For reference : an nMOS Inverter coloured stick diagram



CMOS Inverter Mask Layout

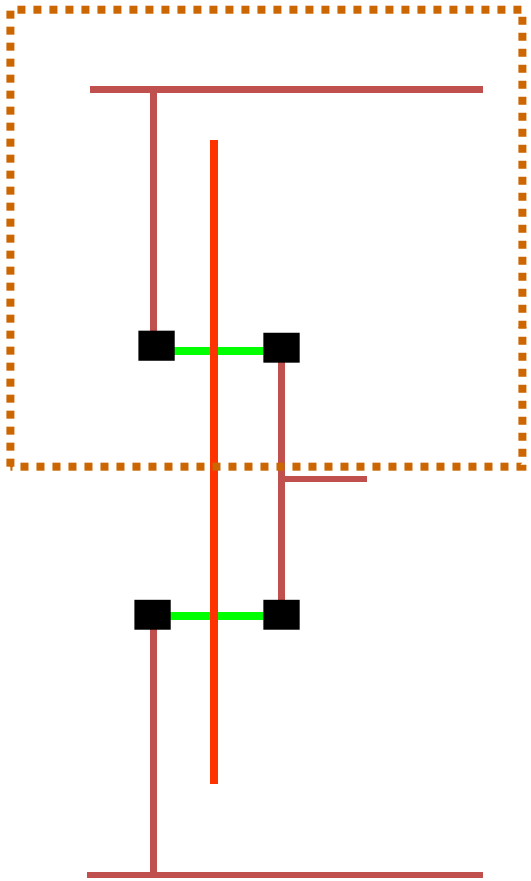


CMOS Inverter Mask Layout



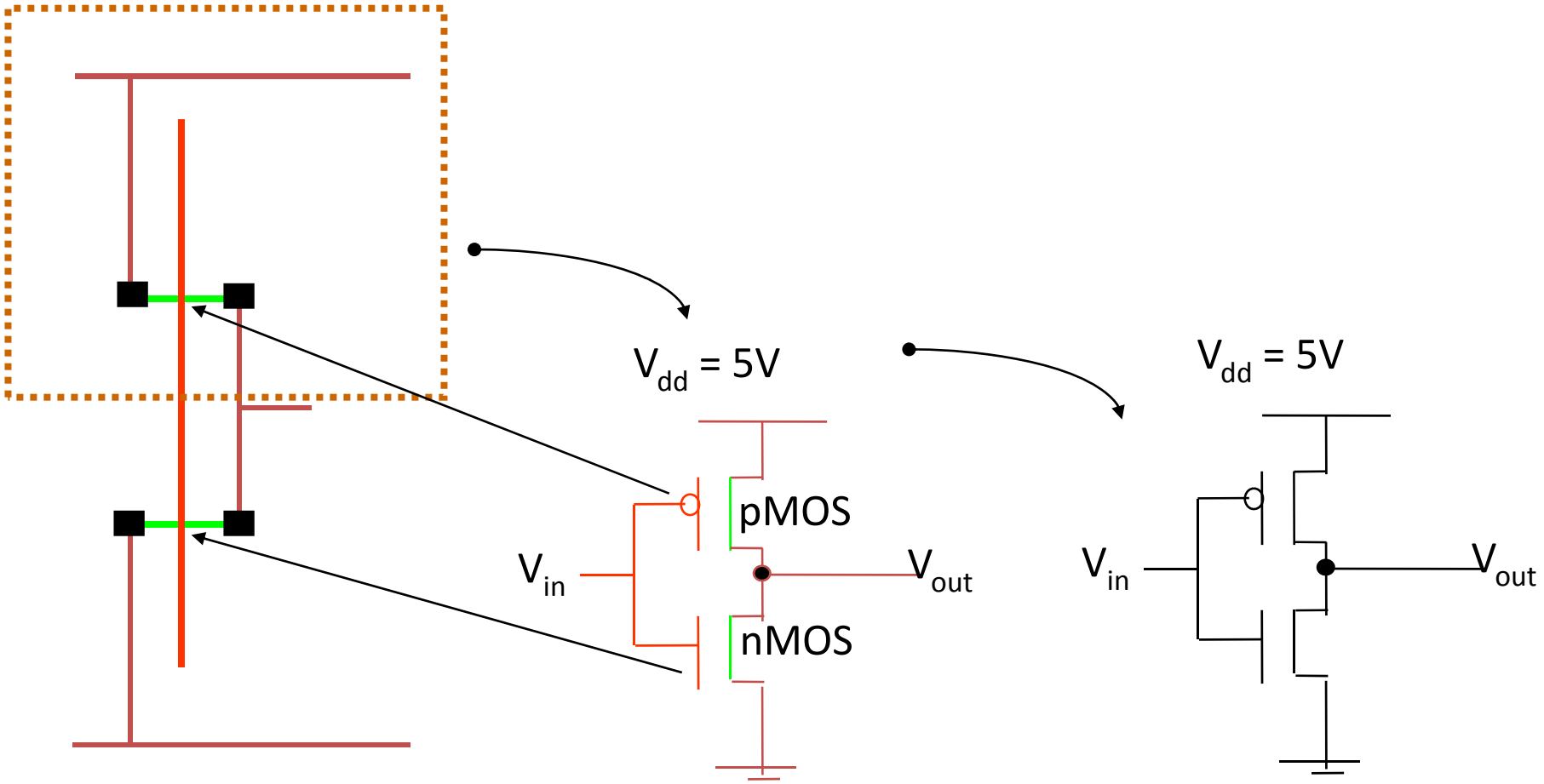
Simplify by deleting connections provided for interconnecting cell (additional pads and output metal rails)

CMOS Inverter coloured stick diagram



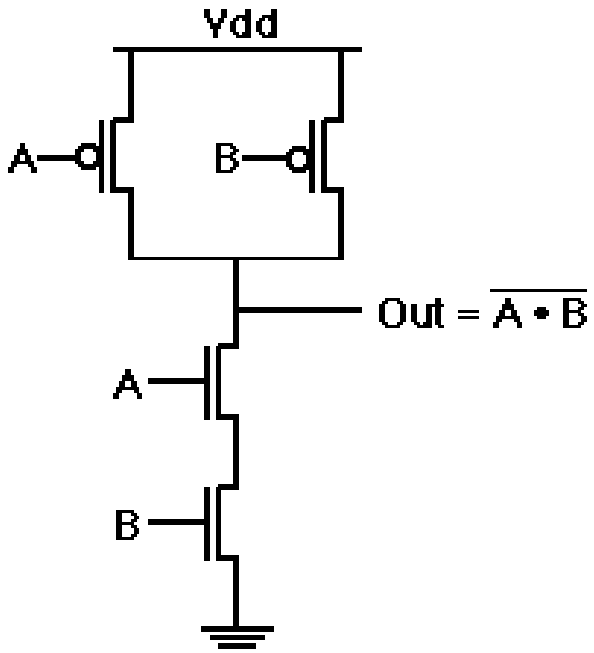
diffusion
polysilicon
metal
contact windows
depletion implant
P well

Stick diagram -> CMOS transistor circuit

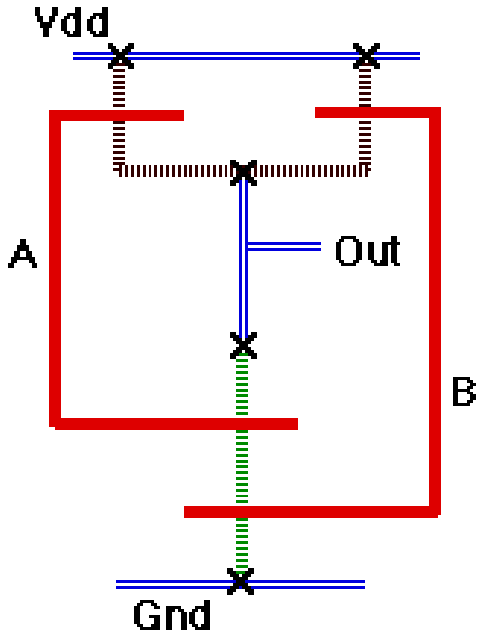


In practice, first draw stick diagram for nMOS section and analyse (pMOS is dual of nMOS section)

Static CMOS NAND gate



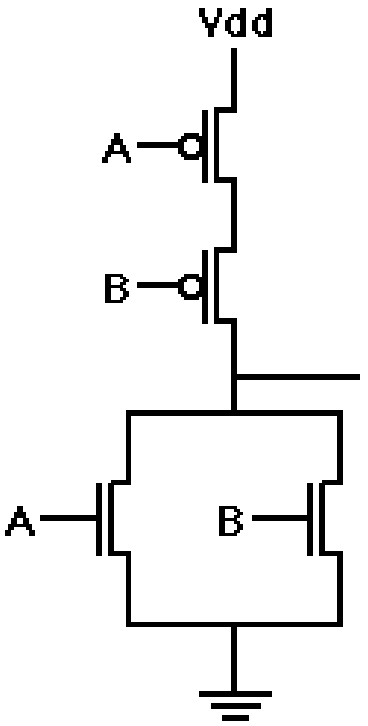
A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0



1. Pull-down: Connect to ground If A=1 AND B=1

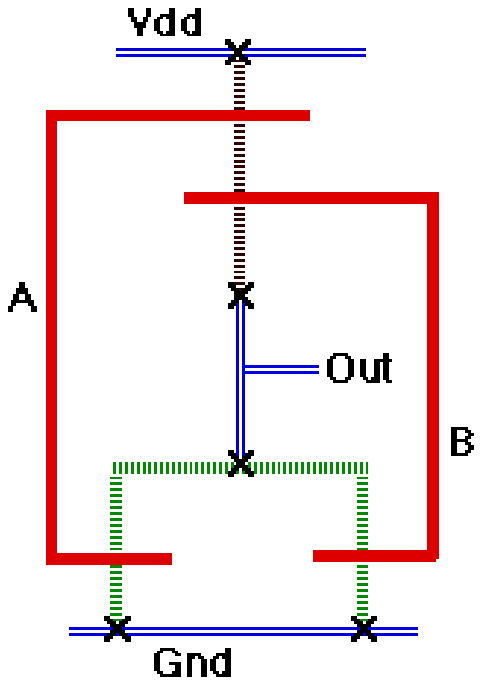
2. Pull-up: Connect to Vdd If A=0 OR B=0

Static CMOS NOR gate



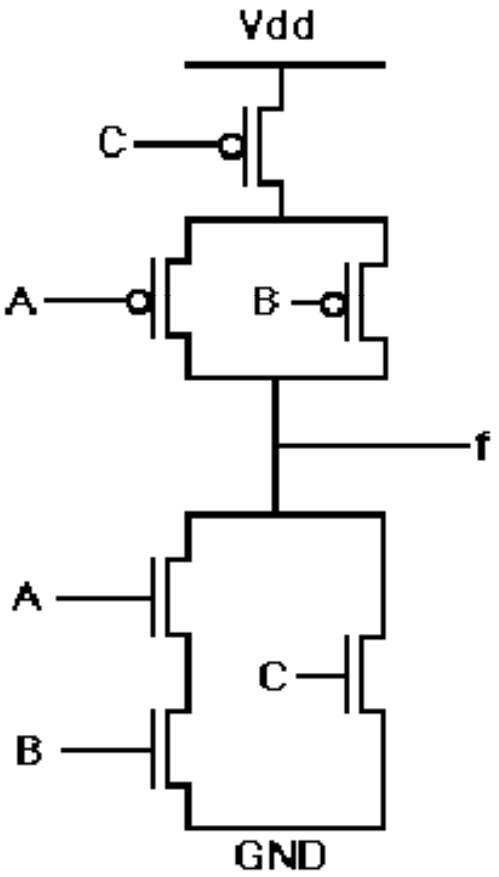
Out = $\overline{A+B}$

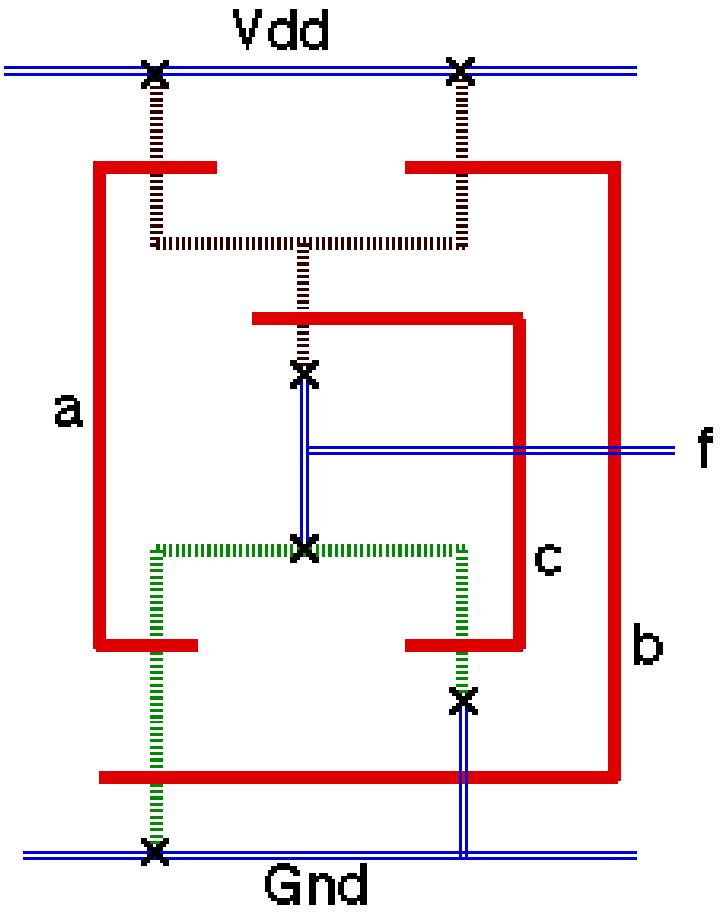
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



1. Pull-down: Connect to ground if A=1 OR B=1
2. Pull-up: Connect to Vdd if A=0 AND B=0

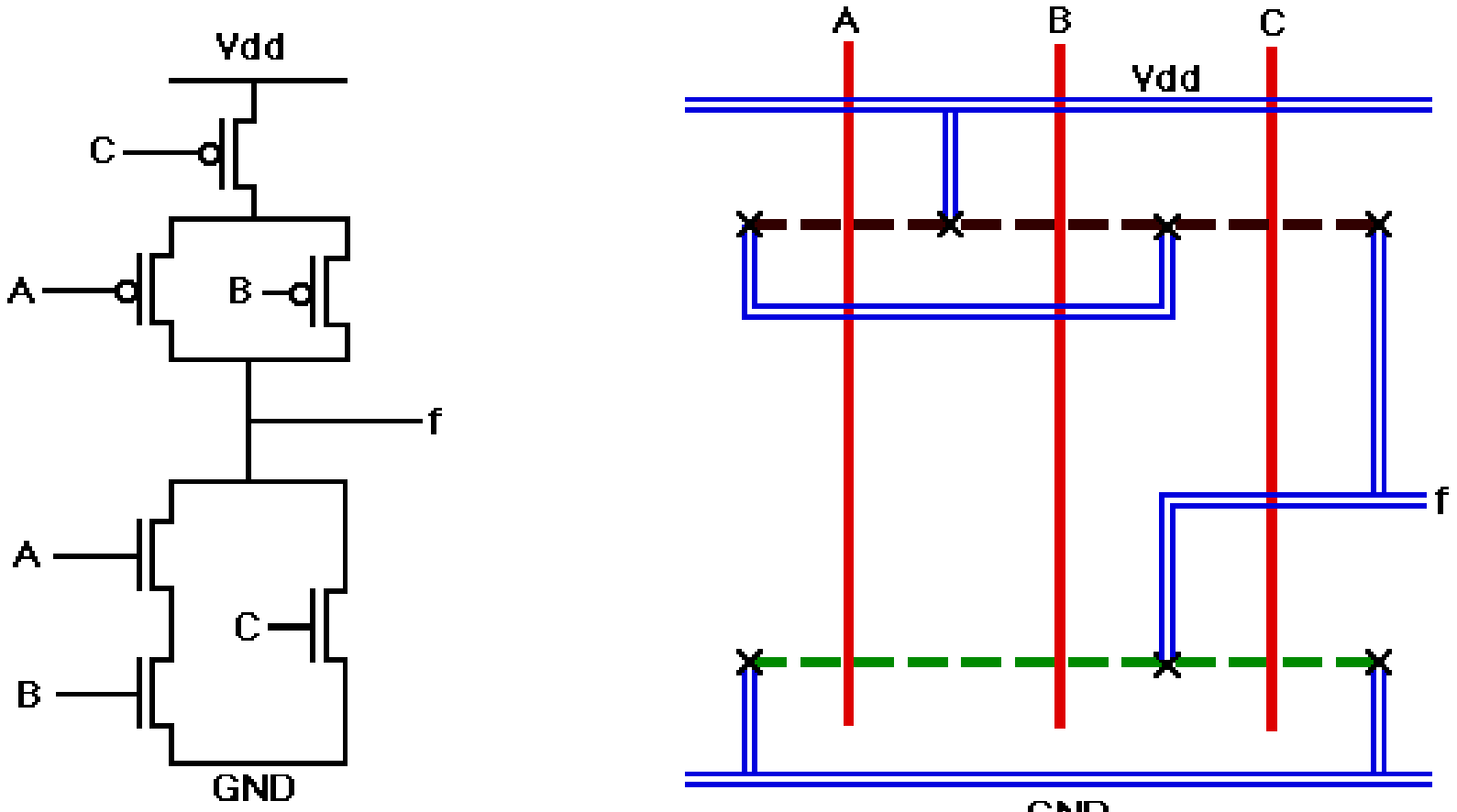
Static CMOS Design Example Layout





Example: $f = \overline{a \cdot b + c}$

Layout 2 (Different layout style to previous but same function being implemented)



Example: $f = \overline{a \cdot b + c}$

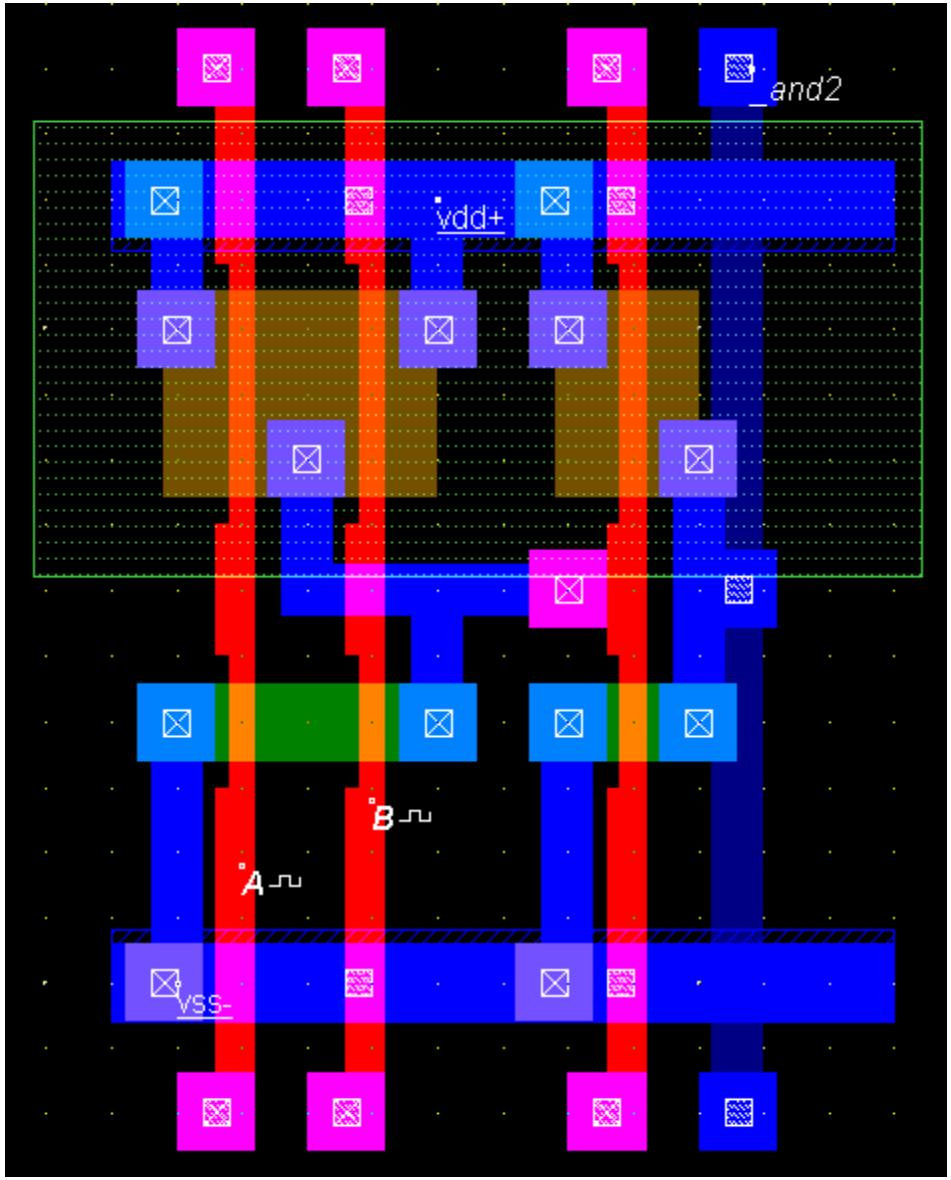
Steps in translating from layout to logic circuit

1. Try to simplify mask layout diagram by removal of extended metal and polysilicon lines

2. First draw coloured stick diagram for nMOS section and analyse
   All nMOS transistor nodes which connect to GND terminal are SOURCE nodes

3. Since the pMOS section is the dual of the nMOS section, draw the pMOS stick diagram and confirm the outcome of step 2.
   All pMOS transistor nodes which connect to Vdd terminal are pMOS SOURCE nodes

Exercise : Draw coloured stick diagram and logic circuit for this CMOS mask layout



Layout Design Rule

$\lambda = 1\mu m$

MINIMUM WIDTH AND SPACING RULES

LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
ACTIVE	Minimum Width Minimum Spacing	3λ 3λ
NSELECT	Minimum Width Minimum Spacing	3λ 3λ
PSELECT	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

MOSFET LAYOUT RULES

RULE	MEANING	VALUE
POLY Overlap	Minimum extension over ACTIVE	2λ
POLY-ACTIVE	Minimum Spacing	1λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
ACTIVE CONTACT	Exact Size Minimum Space to ACTIVE Edge	2λ x 2λ 2λ
POLY CONTACT	Exact Size Minimum Space to POLY Edge	2λ x 2λ 2λ

Double metal single poly CMOS Process

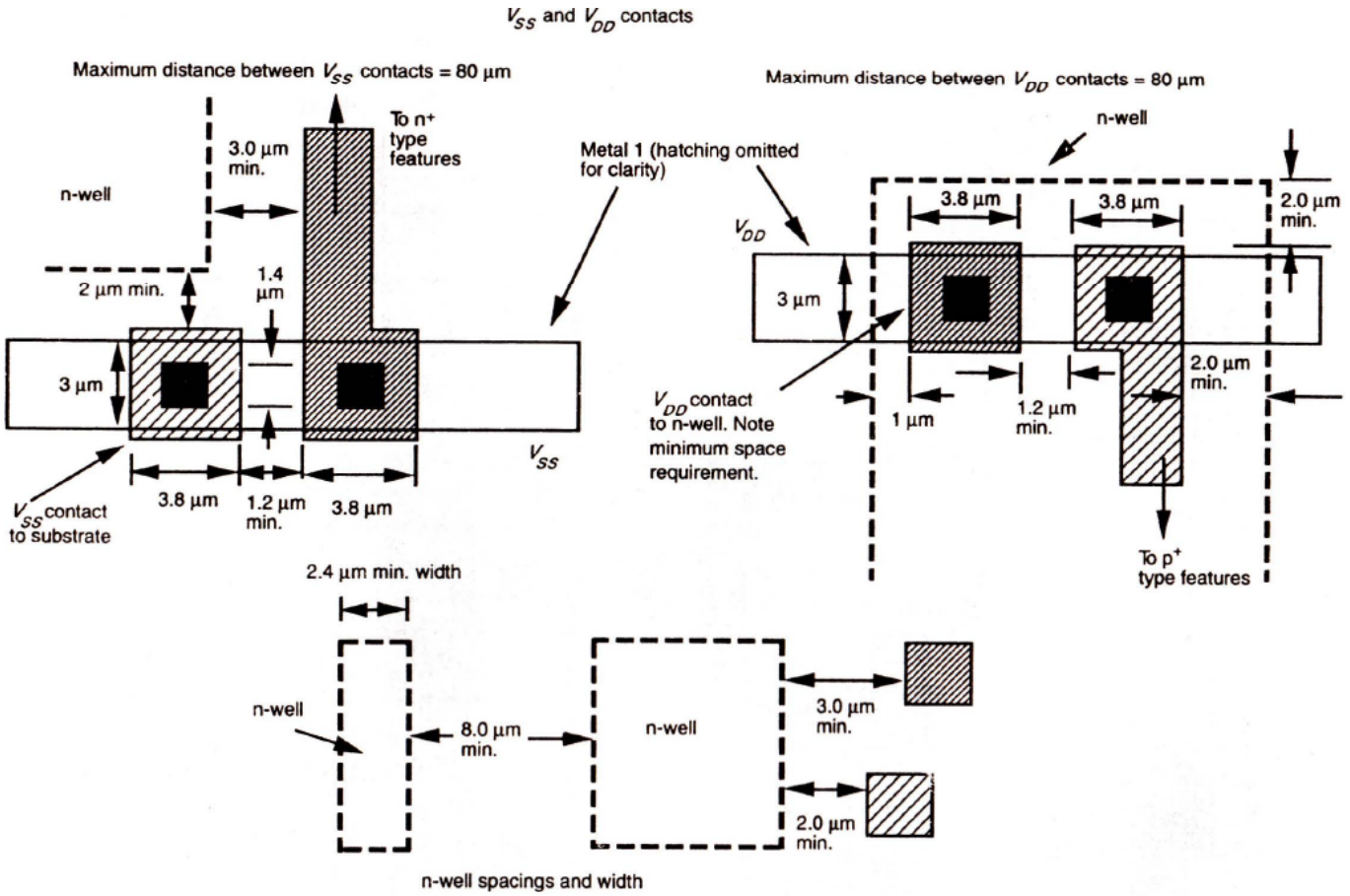


FIGURE B.1(D) Rules for n-well (Orbit 1.2 µm CMOS process).